A High-Speed, 240-Frames/s, 4.1-Mpixel CMOS Sensor

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***Abstract*—This paper describes a large-format 4-Mpixel (2352×1728) sensor with on-chip parallel 10-b analog-to-digital converters (ADCs). The chip size is 20 × 20 mm with a 7-μm pixel pitch. At a 66-MHz master clock rate and 3.3-V operating voltage, it achieves a high frame rate of 240 frames/s delivering 9.75 Gb/s of data with power dissipation of less than 700 mW. The principal architectural features of the sensor are discussed along with the results of sensor characterization.**

***Index Terms*—CMOS image sensor, high-speed imaging, machine vision.**

I. Introduction

CMOS sensors are rapidly advancing in high-speed imaging. Compared to high-speed CCDs, with a degree of parallelism represented by the number of panels, CMOS sensors utilize the natural advantage of a column-parallel readout from the pixels. Row processing time can be readily reduced to 1 μs and lower, and the high-speed design focuses on such challenges as column-multiplexing, analog-to-digital conversion, and the reduction of system noise. Another advantage of a CMOS sensor to CCD is practically no smear nor blooming.

Three years ago, a 1-Mpixel digital image sensor with rolling shutter running at 500 frames/s was presented [1]. It showed an improvement in data rate of an order of magnitude compared to the state-of the art high-speed CMOS sensors. Since that time, the progress was steady, but gave only about a factor of 2 increase in data throughput over three years. Mostly, the efforts were centered on the development of the pixels with a full-frame shutter, featuring competitive performance [2], [3]. We believe that the state-of-the-art in the year 2002 is a 1K × 1K × 1K sensor (1000 frames/s) with a shutter pixel. It is very likely that the progress in high-speed CMOS imaging for many years in a row will still be defined by column-parallel architectures. However, a new generation of digital sensors [4] utilizing a higher, pixel-level degree of parallelism may be an additional path to high-speed image capture.

This paper presents a chip that is a result of the further development of the baseline high-speed digital sensor design [1]. A smaller feature size (0.35 μm) allowed an increase in resolution from 1024×1024 to 2352×1728. Also, column-parallel analog-to-digital converters (ADCs) were upgraded from 8- to 10-b resolution.

The paper is organized as follows. Section II describes key building blocks, Section III discusses the implementation of the sensor, and Section IV presents the characterization results and their discussion. The paper is concluded with a summary and acknowledgment.

II. Sensor Building Blocks

The sensor block diagram is presented in Fig. 1. In addition to the pixel array, the sensor contains column-parallel ADCs and memory, column and row decoders, row drivers, and two controllers to run row operations including A/D conversion and read-write memory operations.

The pixel is a conventional three-transistor APS pixel. No special techniques are needed to design the pixel for a microsecond access time. One exception, perhaps, is the design of control lines for row select and pixel reset. The metal lines for a Megapixel imager have typical resistance/capacitance of the order of 1 kΩ/2 pF, so the settling time for pixel control pulses is within several tens of nanoseconds. However, convenient poly lines, even if silicided, can no longer be used because of a two-order-of-magnitude higher resistance than that of metal lines.

The pixel source-follower is the next speed bottleneck. Rather than pumping more current into the circuit, we clamp the column readout bus to the ground before the pixel is read to benefit from fast operation of the source-follower in one direction, that is, charging the bus. A similar technique was used for the second buffer that charges ADC capacitances.

ADCs used in the chip were the successive-approximation type [5]. This type of ADC was very popular in the first digital active-pixel sensors. The reason for this was the simplicity of the ADC design and their low power. Another useful advantage of digitizing in columns was the higher speed of digital-data multiplexing compared to the multiplexing of column buffer outputs typically used at that time. However, as soon as higher speed analog-readout circuits were developed (an example is [6]), the column-parallel approach was replaced by a single ADC architecture in most consumer CMOS sensors. One motivation for this transition was large area (typically 2–3 mm in height) occupied by the successive-approximation ADC. Another drawback of the first column ADCs was a visible column fixed pattern noise (FPN). Although the ADCs had calibration circuits, they did not completely remove what was believed to be a comparator-to-comparator offset. One of possible reasons was the effect of digital noise from control lines and ADC latches on the

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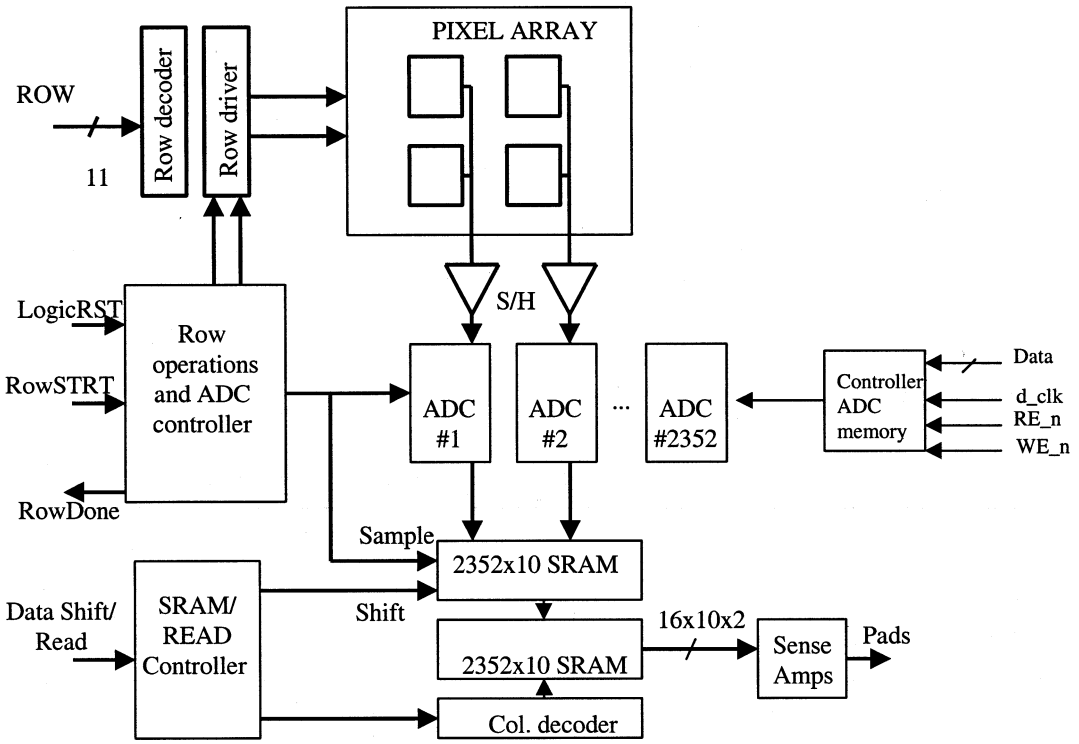

Fig. 1. Block diagram of the sensor.

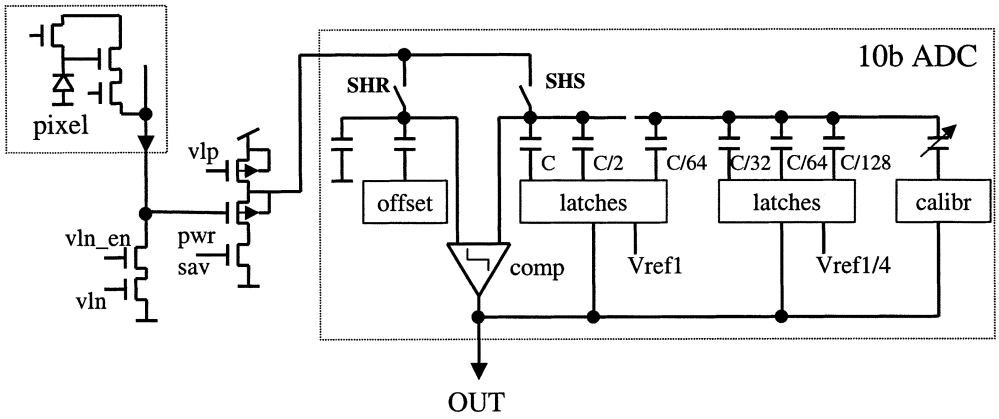

Fig. 2. Schematic of column readout circuit including ADC.

calibration process. Nonetheless, the column-parallel approach has remained very strong in the area of high-speed sensors, and it has undergone several improvements.

First, the memory portion of the ADC and the digital readout were spatially separated from the ADC [1]. (Before, the ADC was structured as the sandwich of (capacitor-latch-readout) slices.) Second, the memory was built as a two-port SRAM: parallel *in* (from ADCs) serial *out*. The front-end memory stored ADC data from the new row of the image and allowed the simultaneous output of the previous row. The present 4-Mpixel chip also has these architectural features. The two memory cells are implemented as SRAM. The readout from SRAM is differential through sense-amps.

In order to reduce column FPN, the comparator design was optimized [7] for less power and smaller offset. It was also decided to fix the convergence voltage for the ADC to remove the possible issue of signal-dependent comparator offset. In such an architecture, a variable signal approaches a fixed voltage, and in no case vice versa. Thus, in the column ADC in Fig. 2, the pixel reset voltage is stored on one capacitor, while the variable pixel signal is applied to the capacitor bank, to be compensated for during the convergence process.

The core of the successive-approximation ADC is the comparator and the binary-scaled conversion capacitors with latches and switches connecting the capacitor either to the ground or to the ADC reference (Vref1 here). One step includes application of the trial voltage, the comparison, and, then, an acceptance or a rejection of the try.

There was an opinion in the literature that the accuracy of binary scaling of passive components is limited to about 8 bits due

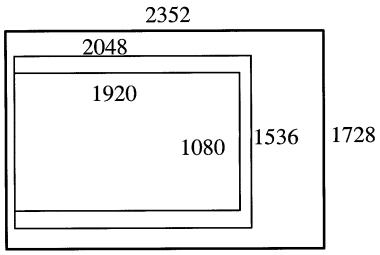

Fig. 3. Resolution supported by the sensor.

to parameter mismatch. Although in reality it may happen to be better, to guarantee a higher ADC resolution we scaled the three smallest capacitors up (by a factor of 4) with concurrent reduction of the reference for these bits to $1/4$ of the ADC reference, in the present design. The requirement to the new reference is not severe ($\pm$7%) because of the small weight of the smallest bits, so the reference can be generated using a simple circuit. (We used a resistive divider of Vref1, with a tap for a decoupling capacitor).

Similar to the conversion capacitor bank, there is a calibration capacitor digital-to-analog converter (DAC), which uses smaller capacitors (the largest calibration capacitor is C/4; here C is the size of the largest conversion capacitor). Each latch in the calibration DAC also has an SRAM cell to store the results of calibration. The earlier 1-Mpixel sensor [1] had a 5-b accuracy offset-calibration circuit that was apparently not sufficient and resulted in column FPN on the order of 1.5 mV rms. In the reported sensor, the DAC resolution was increased to 7 b. In addition, a read/write access to the calibration DACs was provided through a serial interface. The controls to the interface are *read enable*, *write enable*, *data*, and *data clock*. This access yields stability of calibration vectors during the sensor operation (they could be read once and then downloaded again and again, when needed). Also, if for some reason the internal calibration did not fully remove column-wise FPN, the values could be calculated externally and written back into the chip.

A sensor resolution of 2352$\times$1728 elements has a useful aspect ratio of 4:3 and corresponds to 4.1-Mpixel DSC format. Also, the sensor can support a Super XGA (2048$\times$1536) computer format. The chip can be used as a high-speed HDTV imager with a subresolution of 1920$\times$1080 (Fig. 3). The sensor was designed so that row operations are completed in 128 clock cycles. This corresponds to the readout of 2048 columns. Thus, the speed in subresolution modes can be further increased by skipping the unread columns. Of course, this is in addition to the reduction of the frame time with fewer rows in the frame.

Direct external addressing to the rows gives the user a flexibility of selecting the window-of-interest within the center of the pixel array, achieving maximum photoresponse uniformity.

III. Manufacturing

The floorplan of the chip layout is outlined in Fig. 4, with the pixel layout presented in Fig. 5. ADCs and memory are split between the top and the bottom for symmetry, performance, and routing considerations. Digital pads are on the left and at the top/bottom. Analog pads are to the right.

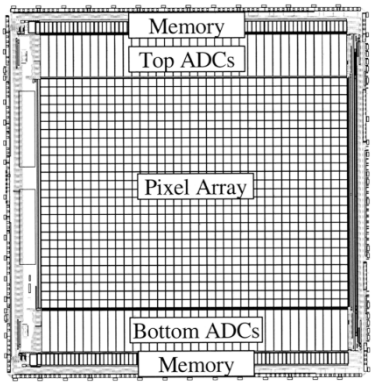

Fig. 4. Floorplan of the chip.

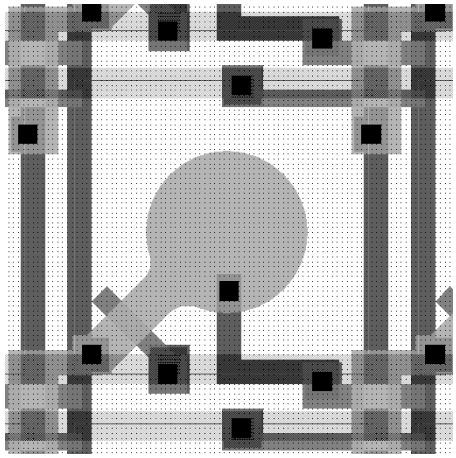

Fig. 5. Pixel layout.

The pixel array area slightly exceeds a $1''$ format, which makes convenient use of 35-mm optics, although we found some $1''$ lenses that are also applicable. The chip, with a size of 19.8 mm $\times$ 19.8 mm, fits into one reticule.

Wafers were fabricated in the 0.35-μm United Microelectronics Corporation CMOS sensor process with double-poly used for capacitors, triple-metal for routing, and a lightly doped substrate left in the area of the pixel array.

IV. Characterization Results

The sensor was characterized using a custom board with a frame grabber and a PC interface. The board provided 10 bits of image recording. All the measurements were performed for the sensor running at 130 frames/s and for ADC reference voltage of 1 V. The results of the characterization are summarized in Table I. The parameters in volts and electrons are referred to the pixel's floating diffusion.

Fig. 6 shows the square of noise as a function of signal. This is a typical measurement of the conversion gain. From this plot, the conversion gain at the ADC output was 0.045 b/e^-.

Fig. 7. shows quantum efficiency (QE) measurement results with 43% QE at 550 nm. The sensor also demonstrates good response in blue and red.

The 7-μm pixel shows quantum efficiency similar to the 10-μm prototype [1]. This is due to tighter design rules and

TABLE I
SUMMARY OF THE SENSOR CHARACTERIZATION

Technology	0.35um 2P3M
Resolution	2352x1728
Maximum frame rate	240 Frames/s
Pixel pitch	7um
Responsivity @550nm	2.5 V/Lux-s
QE*FF @550nm	43%
Noise, r.m.s.	1.2 lsb or 26e-
DSNU, r.m.s.	2.7 lsb or 60e-
PRNU at 1/2 sat, r.m.s.	10 lsb or 1%
Conversion gain	39 uV/e
Dynamic range @1V ADC reference	59 dB
ADC	10 bit
Number of outputs	16 x 10 bit
Power supply	3.3V
Power	<700 mW
Package	280 PGA

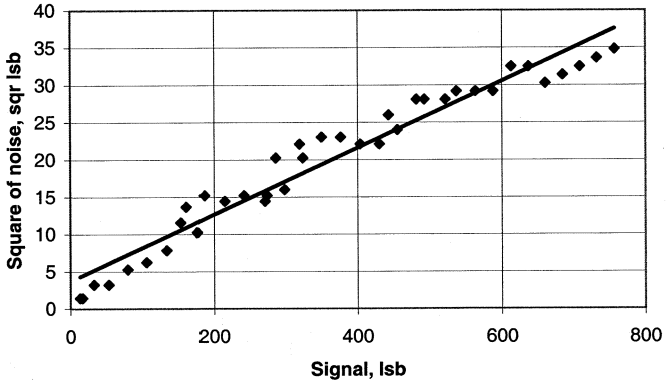

Fig. 6. Conversion gain measurements.

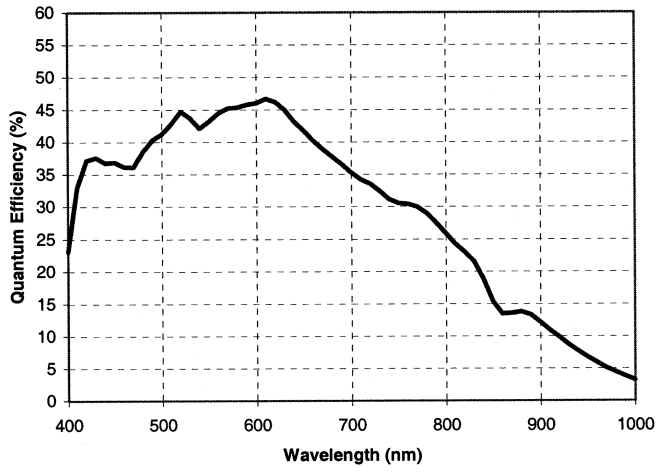

Fig. 7. Quantum efficiency.

the use of the specialized 0.35-μm CMOS sensor process with improved collection. The photodiode capacitance was reduced by approximately a factor of 4. This resulted in a substantial increase of the conversion gain from 11 to 39 $\mu V/e^-$. The Volt/Lux-s responsivity, which is proportional to the pixel size, quantum efficiency, and the conversion gain, grew approximately two times.

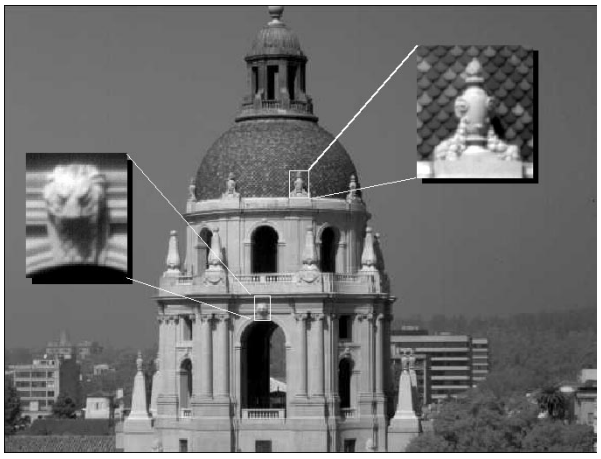

Fig. 8. Image of Pasadena City Hall.

The fundamental noise from the pixel is kTC noise. A smaller photodiode capacitance in the 7-μm pixel provided a factor-of-2 less kTC noise. The previous 1-Mpixel sensor had an excessive electronic noise at 500 frames/s approaching $120e^-$ if the image went through a massive major bit transition. In the new reported sensor, the readout noise was reduced below pixel kTC noise. Dark FPN (which also included "frozen" temporal noise from ADC calibration) is $60e^-$ rms without the additional FPN correction circuit. This is compared to a $200e^-$ FPN in [1]. However, the noise converted into volts is comparatively slightly worse because of much higher conversion gain. The total (temporal + spatial) noise for the prototype was 2.3 mV and for the new sensor 2.7 mV.

The sensitivity of the reported sensor, which can be defined as the reciprocal of the minimum exposure needed to achieve a signal-to-noise ratio (SNR) of 10, is thus the responsivity (in [V/Lux-s]) divided by the tenfold total noise (in [V]), and it is 70% higher than in the prototype. The minimum light needed to achieve such a threshold SNR for the 4-Mpixel sensor operating without the lens at the maximum frame rate of 240 frames/s would be 2.5 Lux.

Previously, a higher temporal noise ($50e^-$) and the spatial noise ($90e^-$) from this sensor was reported [8]. It was, however, found that the pixel reset pulse generated on the chip was boosted too much and caused the "hard" reset of the pixels [9]. The sensor could be turned into the less noise "soft" reset mode by either lowering digital VDD voltage to 2.9 V or by increasing pixel VDD voltage to 3.8 V.

To avoid excessive image lag, the chip has the capability of a flushed-reset mode, which is a combination of hard and soft reset, similar to the one described in [9].

The dynamic range was 59 dB at 1 V ADC reference and the overall data rate delivered by the sensor at the maximum frame rate approaches almost 10 Gb/s. A sample image taken with the sensor is shown in Fig. 8.

There are several important applications for a high-speed sensor without a parallel (or "freeze-frame") shutter even though a rolling shutter is known to introduce motion distortion. These applications include

- strobe light illumination of the scene;

- predictable motion so that the distortion can be software-corrected;
- when there is no alternative;
- when high-speed operation gives better scene sampling than lower speed operation with a freeze-frame shutter.

For example, the uncertainty in timing acquisition due to a rolling shutter for this sensor is ∼5 ms at 200 frames/s. Then, the image distortion should be indistinguishable from the inherent motion-blur if the shutter speed is less that 1/250 s.

V. Conclusion

A high-speed 4-Mpixel CMOS sensor and the results of its characterization are reported in this paper. The sensor targets the high-speed camera market and scientific and machine vision applications and can also be used for high-speed HDTV.

Future work should concentrate on the reduction of the chip optical format and on the shuttered version of the pixel.

Acknowledgment

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Alexander I. Krymski (M'97) graduated from Novosibirsk University, Novosibirsk, Russia, in 1984 and received the Ph.D. degree from the Institute for Semiconductor Physics, Novosibirsk, in 1992, where he worked on a photo-electrical characterization of MOS devices, and CCD/CMOS multiplexers for infrared focal plane arrays.

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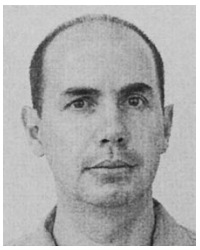

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From 1998 to 2001, he was with Photobit Corporation as the lead designer on high-volume CMOS APS image sensors for PC and digital still cameras, as well as working on high-speed, high-resolution sensors for machine vision. In 2001, he joined Forza Silicon Corporation, Pasadena, CA, as its Chief Technology Officer, where he is developing multigigabit transmitters and receivers for parallel optical modules and specialized sensor ICs.

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As a member of Columbia University's Electrical Engineering faculty from 1984-1990, he and his students performed research on CCD focal-plane image processing and high speed III-V CCDs. In 1990, Dr. Fossum joined the NASA Jet Propulsion Laboratory, California Institute of Technology, Pasadena, and managed JPL's image sensor and focal-plane technology research and advanced development. He led the invention and development of CMOS active pixel sensor (APS) camera-on-a-chip and subsequent transfer of the technology to US industry. In 1996, he joined Photobit Corporation as Chief Scientist, a company he helped found in 1995, and became CEO of Photobit Technology Corporation in 2000. While at Photobit, he and his staff commercialized the camera-on-a-chip which has been used in Logitech® and Intel® PC cameras, ultra-low-power sensors enabling the swallowable "pill-camera", and very-high-speed, high-resolution sensors used for Hollywood special effects such as in *The Mummy Returns* and *Pearl Harbor*. In late 2001, Photobit was acquired by Micron Technology, Inc. and he is presently a Senior Micron Fellow. He has also served as Adjunct Professor of electrical engineering at the University of California, Los Angeles (UCLA), and is currently Adjunct Professor of electrical engineering-electrophysics at the University of Southern California (USC), Los Angeles, and teaches undergraduate physical electronics. He has served as primary adviser to 12 Ph.D. candidates. He has published 230 technical papers and holds 53 U.S. patents.

Dr. Fossum received Yale's Becton Prize in 1984, the IBM Faculty Development Award in 1984, the National Science Foundation Presidential Young Investigator Award in 1986, the JPL Lew Allen Award for Excellence in 1992, and the NASA Exceptional Achievement Medal in 1996. He was inducted into the U.S. Space Foundation Technology Hall of Fame in 1999. He founded the biannual IEEE Workshops on CCDs and Advanced Image Sensors and the SPIE Conferences on Infrared Readout Electronics. He has served on program committees for the IEDM, ISSCC, and SPIE conferences. He has served as associate editor for IEEE TRANSACTIONS ON VLSI, guest editor for IEEE JOURNAL OF SOLID STATE CIRCUITS, and was Guest Editor-in-Chief for IEEE TRANSACTIONS ON ELECTRON DEVICES Special Issue on Solid-State Image Sensors published in October 1997. He was recently named to the Board of Fellows for Trinity College, where he also serves on the college's Engineering Advisory Committee.